Refine Search

Search Results -

Terms	Documents
invert$4 same data same (mask$3 near5 (pin or terminal))	73

Database:
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Search History

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Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	invert$4 same data same (mask$3 near5 (pin or terminal))	73	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
L1	0

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Search: L2

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Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	L1	0	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	invert$4 same data same (mask$3 near5 (pin or terminal))	73	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
(377/41 |710/100 |710/305 |710/52 |710/72 |365/189.01 |365/189.07 |326/21 |326/52 |326/62).ccls.	8685

Database:
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- JPO Abstracts Database
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Search: L3

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, January 26, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	710/100,305,52,72;377/41;326/21,52,62;365/189.01,189.07.ccls.	8685	L3
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	L1	0	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	invert$4 same data same (mask$3 near5 (pin or terminal))	73	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and L3	8

Database:
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US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, January 26, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L4	l1 and L3	8	L4
L3	710/100,305,52,72;377/41;326/21,52,62;365/189.01,189.07.ccls.	8685	L3
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	L1	0	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	invert$4 same data same (mask$3 near5 (pin or terminal))	73	L1

END OF SEARCH HISTORY

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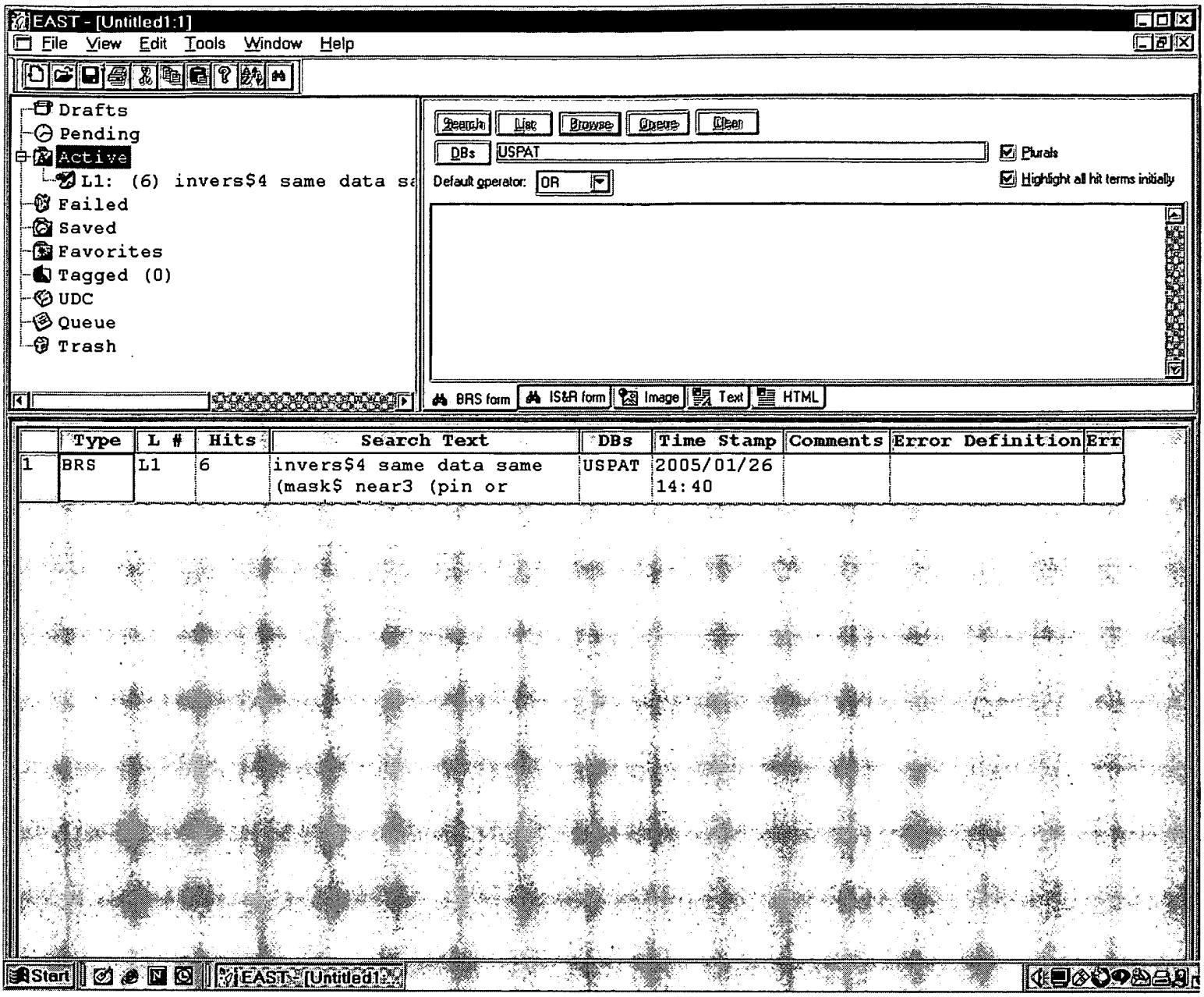
EAST - [Untitled1:1]
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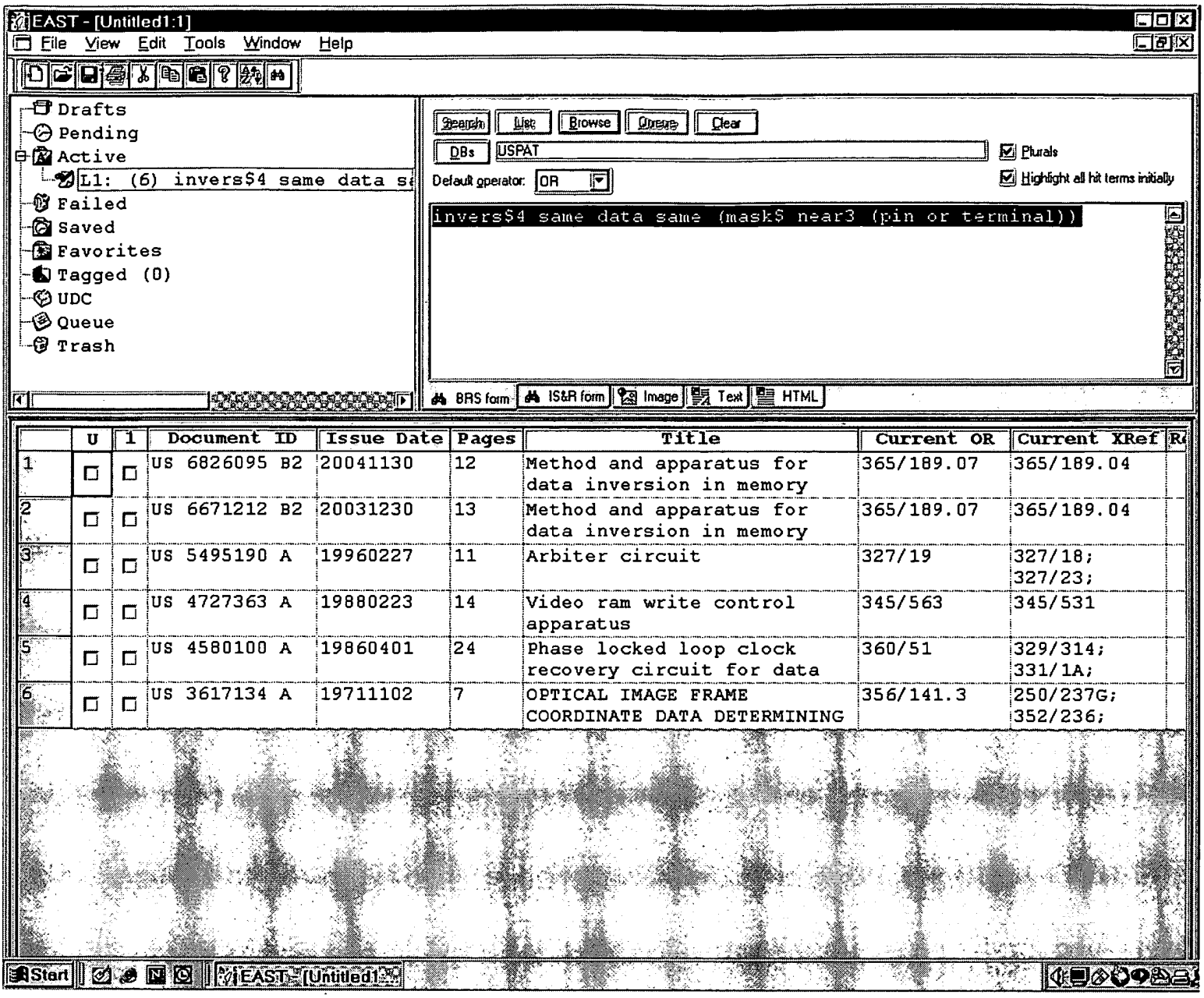

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 6826095 B2	20041130	12	Method and apparatus for data inversion in memory	365/189.07	365/189.04	
2	☐	☐	US 6671212 B2	20031230	13	Method and apparatus for data inversion in memory	365/189.07	365/189.04	
3	☐	☐	US 5495190 A	19960227	11	Arbiter circuit	327/19	327/18; 327/23;	
4	☐	☐	US 4727363 A	19880223	14	Video ram write control apparatus	345/563	345/531	
5	☐	☐	US 4580100 A	19860401	24	Phase locked loop clock recovery circuit for data	360/51	329/314; 331/1A;	
6	☐	☐	US 3617134 A	19711102	7	OPTICAL IMAGE FRAME COORDINATE DATA DETERMINING	356/141.3	250/237G; 352/236;	

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Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

invert* and data and mask<and>(pin or terminal) Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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Results:
No documents matched your query.

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invert* and data and mask* Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Evaluation of the MODIS vegetation index compositing algorithm us SeaWiFS data**
van Leeuwen, W.J.D.; Huete, A.R.; Laing, T.W.;
Geoscience and Remote Sensing Symposium Proceedings, 1998. IGARSS '98. IEEE International , Volume: 3 , 6-10 July 1998
Pages:1445 - 1447 vol.3

[Abstract] [PDF Full-Text (408 KB)] IEEE CNF

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2 **Enhanced biclustering on expression data**
Jiong Yang; Haixun Wang; Wei Wang; Yu, P.;
Bioinformatics and Bioengineering, 2003. Proceedings. Third IEEE Symposium on , 10-12 March 2003
Pages:321 - 327

[Abstract] [PDF Full-Text (404 KB)] IEEE CNF

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3 **Interval estimation from censored and masked system-failure data**
Doganaksoy, N.;
Reliability, IEEE Transactions on , Volume: 40 , Issue: 3 , Aug. 1991
Pages:280 - 286

[Abstract] [PDF Full-Text (500 KB)] IEEE JNL

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4 **M nit ring detailed land surface changes using an airb rne multisp digital camera system**
Stow, D.; Hope, A.; Nguyen, A.T.; Phinn, S.; Benkelman, C.A.;
Geoscience and Remote Sensing, IEEE Transactions on , Volume: 34 , Issue: 5 , Sept. 1996
Pages:1191 - 1203

[Abstract] [PDF Full-Text (1780 KB)] IEEE JNL

5 **A versatile functi n generat r chip implemented in an I/SUP 2/L ga array**
Bahraman, A.; Levie, J.H.; Chang, S.Y.S.; Hopkins, M.A.; Hartmann, R.A.; Sr J.R.;
Solid-State Circuits, IEEE Journal of , Volume: 17 , Issue: 4 , Aug 1982
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6 **Inversion of modified beamformed array data**
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[Abstract] [PDF Full-Text (136 KB)] IEEE CNF

7 **Integrated detectors for embedded optical interconnections on elec boards, modules, and integrated circuits**
Sang-Yeon Cho; Sang-Woo Seo; Brooke, M.A.; Jokerst, N.M.;
Selected Topics in Quantum Electronics, IEEE Journal of , Volume: 8 , Issue: 6 , Nov.-Dec. 2002
Pages:1427 - 1434

[Abstract] [PDF Full-Text (538 KB)] IEEE JNL

8 **2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)**

Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on , Volume: 2 , 26-29 May 2002
[Abstract] [PDF Full-Text (9198 KB)] IEEE CNF

9 **Inverted thin-film transistors with a simple self-aligned lightly dope drain structure**
Liu, C.-T.; Yu, C.-H.D.; Kornblit, A.; Lee, K.-H.;
Electron Devices, IEEE Transactions on , Volume: 39 , Issue: 12 , Dec. 1992
Pages:2803 - 2809

[Abstract] [PDF Full-Text (700 KB)] IEEE JNL

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Integrated detectors for embedded optical interconnections on electrical boards, modules, and integrated circuits

Sang-Yeon Cho Sang-Woo Seo Brooke, M.A. Jokerst, N.M.
Nat. Sci. Found. Packaging Res. Center, Georgia Inst. of Technol., Atlanta, GA
This paper appears in: **Selected Topics in Quantum Electronics, IEEE J u**

Publication Date: Nov.-Dec. 2002
On page(s): 1427 - 1434
Volume: 8 , Issue: 6
ISSN: 1077-260X
Inspec Accession Number: 7517919

Abstract:
Significant opportunities exist for optical interconnections at the board, modu level if compact, low-loss, high-**data**-rate optical interconnections can be inte these electrical interconnection systems. To create such an integrated optoelectronic/electronic microsystem, **mask**-based alignment of the optical interconnection waveguide, optoelectronic active devices, and interface circuit attractive from a packaging alignment standpoint. This paper describes an int process for creating optical interconnections which can be integrated in a post format onto standard boards, modules, and integrated circuits. These optical interconnections utilize active thin-film optoelectronic components embedded waveguide/interconnection substrate, thus eliminating the need for optical be elements and their alignment, and providing an electrical output on the subst an optical interconnection. These embedded optical interconnections are repo using BCB polymer optical waveguides with embedded InGaAs-based thin-film metal-semiconductor-metal (I-MSM) photodetectors on an Si substrate. These interconnections have been fabricated and tested, and the coupled optical sig waveguide to the embedded photodetector was theoretically modeled at 56.4 was supported by an experimental estimate of 47.8%. The measured full-wid maximum of the electrical pulse from the MSM photodetector embedded in th waveguide was 16.73 ps for an input 500-fs optical laser pulse.

Index Terms:
III-V semiconductors gallium arsenide indium compounds integrated circuit packagin optoelectronics metal-semiconductor-metal structures optical films optical interconne

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optical planar waveguides optical polymers photodetectors substrates 16.73 ps 5(polymer optical waveguides InGaAs InGaAs-based thin-film **inverted** metal-semicond photodetectors MSM photodetector Si Si substrate active thin-film optoelectronic cc electrical boards electrical interconnection systems electrical output electrical pulse optical interconnections embedded photodetector high-**data**-rate optical interconnectic integrated circuits integrated detectors interface circuits microsystem modules opt turning elements optical interconnection waveguide optical interconnections optical l optical testing optoelectronic active devices packaging alignment postprocessing waveguide/interconnection substrate

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Documents that cite this document
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L4: Entry 1 of 8 File: PGPB Aug 21, 2003

PGPUB-DOCUMENT-NUMBER: 20030158981
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030158981 A1

TITLE: Memory bus polarity indicator system and method for reducing the affects of simultaneous switching outputs (SSO) on memory bus timing

PUBLICATION-DATE: August 21, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
LaBerge, Paul A.	Shoreview	MN	US	

APPL-NO: 10/ 081652 [PALM]
DATE FILED: February 21, 2002

INT-CL: [07] G06 F 13/00

US-CL-PUBLISHED: 710/100
US-CL-CURRENT: 710/100

REPRESENTATIVE-FIGURES: 3

ABSTRACT:

A method and system transfer read data from a memory device having a data bus and a data masking pin adapted to receive a masking signal during write operations of the memory device. The method includes placing a sequence of read data words on the data bus and applying a data bus inversion signal on the data masking pin, the data bus inversion signal indicating whether the data contained each read data word has been inverted. Another method and system transfer data over a data bus. The method includes generating a sequence of data words, at least one data word including data bus inversion data. The sequence of data words is applied on the data bus and is thereafter stored. The data bus inversion data is applied to invert or not invert the data contained in the stored data words.

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L4: Entry 8 of 8 File: USPT Feb 28, 1995

US-PAT-NO: 5394366
DOCUMENT-IDENTIFIER: US 5394366 A

TITLE: Enabling data access of a unit of arbitrary number of bits of data in a semiconductor memory

DATE-ISSUED: February 28, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Miyamoto; Takayuki	Hyogo			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Mitsubishi Denki Kabushiki Kaisha	Tokyo			JP	03

APPL-NO: 07/ 925152 [PALM]
DATE FILED: August 6, 1992

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	3-200278	August 9, 1991

INT-CL: [06] G11 C 7/00

US-CL-ISSUED: 365/195; 365/196, 365/193, 365/189.01, 365/189.03
US-CL-CURRENT: 365/195; 365/189.01, 365/189.03, 365/193, 365/196

FIELD-OF-SEARCH: 365/195, 365/189.01, 365/196, 365/221, 365/189.02, 365/189.03, 365/189.12, 365/230.02, 365/230.09, 365/193, 364/514, 364/516

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4669064	May 1987	Ishimoto	365/195
☐	4897818	January 1990	Redwine et al.	365/195
☐	5313624	May 1994	Harriman et al.	395/575

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OTHER PUBLICATIONS

"Home VTR Containing Field Memory for Correcting Crossbar and Skew Distortion in Search Mode", Nikkei Electronics, vol. 406, Oct. 20, 1986, pp. 195-214.

ART-UNIT: 251

PRIMARY-EXAMINER: LaRoche; Eugene R.

ASSISTANT-EXAMINER: Hoang; Huan

ATTY-AGENT-FIRM: Lowe, Price, LeBlanc & Becker

ABSTRACT:

A DRAM device includes a read control circuit for inhibiting read out of one or more bits of a multi-bit data output from a plurality of memory cells in response to a bit designating signal for specifying the one or more bits. By arbitrarily setting the number of bits to be output from the DRAM device and combining that output with data from one or more additional memory devices, data of an arbitrary number of bits can be generated at a high speed.

13 Claims, 17 Drawing figures

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L5: Entry 1 of 1 File: USPT Mar 30, 2004

US-PAT-NO: 6714460
DOCUMENT-IDENTIFIER: US 6714460 B2

TITLE: System and method for multiplexing data and data masking information on a data bus of a memory device

DATE-ISSUED: March 30, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
LaBerge; Paul A.	Shoreview	MN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Micron Technology, Inc.	Boise	ID			02

APPL-NO: 10/ 081653 [PALM]
DATE FILED: February 21, 2002

INT-CL: [07] G11 C 7/00

US-CL-ISSUED: 365/189.01; 365/195
US-CL-CURRENT: 365/189.01; 365/195

FIELD-OF-SEARCH: 365/189.01, 365/195, 365/230.06, 365/235

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5539430	July 1996	Priem et al.	345/545
☐	5657287	August 1997	McLaury et al.	365/230.01
☐	6011727	January 2000	Merritt et al.	365/189.02
☐	6269103	July 2001	Laturell	370/458

ART-UNIT: 2824

h e b b g e e e f c e e ge

PRIMARY-EXAMINER: Le; Vu A.

ATTY-AGENT-FIRM: Dorsey & Whitney LLP

ABSTRACT:

A method and system masking data being written to a memory device having a data bus. One method includes applying masking data on the data bus, storing the masking data in the memory device, applying write data on the data bus, storing the write data in the memory device, and applying the stored masking data to mask the stored write data.

53 Claims, 4 Drawing figures

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Macri et al.

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(54) **METHOD AND APPARATUS FOR DATA INVERSION IN MEMORY DEVICE**

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(52) U.S. Cl. 365/189.07; 365/189.04
(58) Field of Search 365/189.07, 189.04, 365/189.08; 711/167, 202

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(57) **ABSTRACT**

A method of writing information to a synchronous memory device by examining a present word of N bits to be written, where each bit has a high or low value. The present word is compared to a previous word also having N bits to identify the number of bit transitions from a low value to a high value of vice versa. The present bit is inverted when the number of bit transitions is greater than N/2. To avoid the need for having an extra bit accompany data bytes to indicate the presence or absence of inversion, the present invention takes advantage of a data mask pin that is normally unused during writing operations to carry the inversion bit. Non-inverted data is written directly into the memory device while inverted data is first inverted again before writing to storage locations, so that true data is stored in the memory device.

29 Claims, 7 Drawing Sheets